

D-A and A-D Converters...

Introduction :-

- * Most of the information carrying signals such as voltage, current, charge, temperature, pressure and storage time are available in the analog form.
- * However, for processing, transmission and storage process, it is often more convenient to express such signals in the digital form.
- * When expressed in the digital form, they provided better accuracy and reduce noise.
- * Digital systems such as microprocessor use a binary system of ones and zeros, we have to convert signal from analog to digital (A/D) converter.
- * Digital to Analog (D/A) converter is used in when a binary output from a digital system must be converted to some equivalent analog voltage or current.

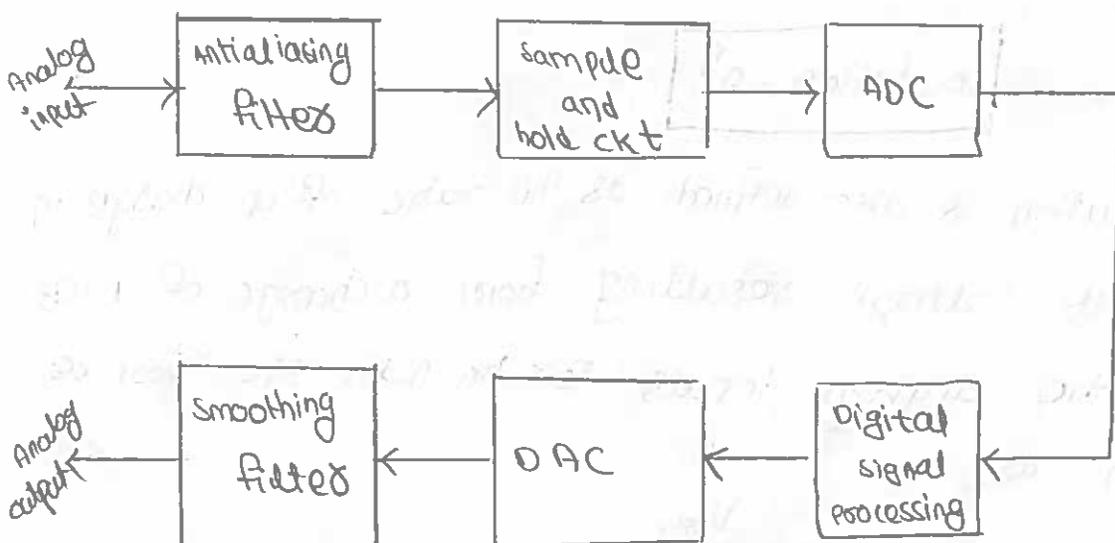


Fig :- Typical A/D & D/A converter

Digital to Analog Converters :-

- A DAC (Digital to Analog converter) accepts an n -bit input word $b_1, b_2, b_3, \dots, b_n$ in binary and produce an analog signal proportional to it.
- In DAC there are four digital inputs, indicating 4-bit DAC.
- Each digital input requires an electrical signal representing either a logic 1 or logic 0.
- The b_n is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB.

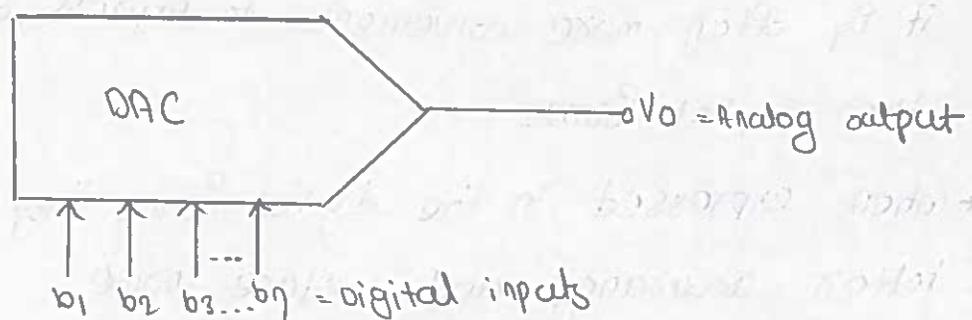


Fig:- DAC circuit symbol.

Performance Parameters specifications of DAC :-

The various performance parameters of DAC are,

1. Resolution :-

Resolution is defined in two ways

- * Resolution is the number of different analog output values that can be provided by a DAC. For an n -bit DAC.

$$\text{Resolution} = 2^n$$

- * Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n -bit DAC it can be given as

$$\text{Resolution} = \frac{V_{\text{FS}}}{2^n - 1}$$

2. Accuracy :-

It is a comparison of actual output voltage with expected output. It is expressed in percentage.

$$\text{Accuracy} = \frac{V_{\text{ofs}}}{(2^n - 1) \Delta}$$

3. settling Time :-

The operating conversion speed of a DAC is usually specified by giving its settling time. The settling time is the time required for the DAC output to go from zero to full scale as the binary input is changed from all 0s to all 1s.

4. Dynamic Range :-

The dynamic range of DAC is defined as the ratio of the largest output to the smallest output, excluding zero. It is expressed in dB. For linear DACs it is given by

$$\text{Dynamic range} = 20 \log_2 2^n \approx 6n$$

5. Offset Error :-

The offset error is defined as the nonzero level of the output voltage when all inputs are zero.

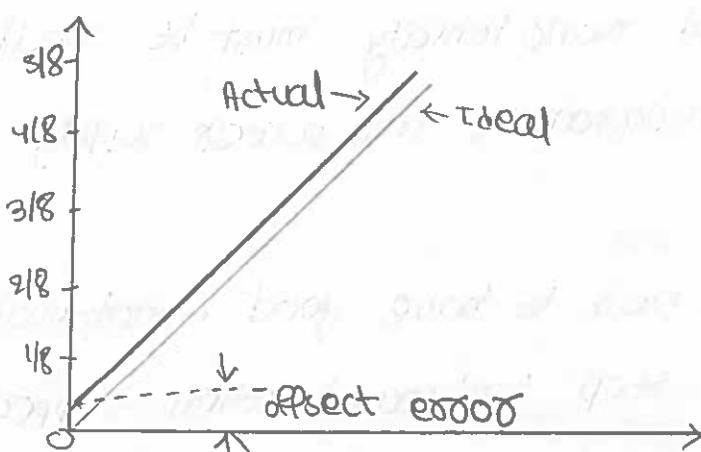


Fig:- offset error in transfer

characteristics of DAC

6. Gain error :-

The gain error is defined as the difference b/w the calculated gain of the current to voltage converter and the actual gain achieved.

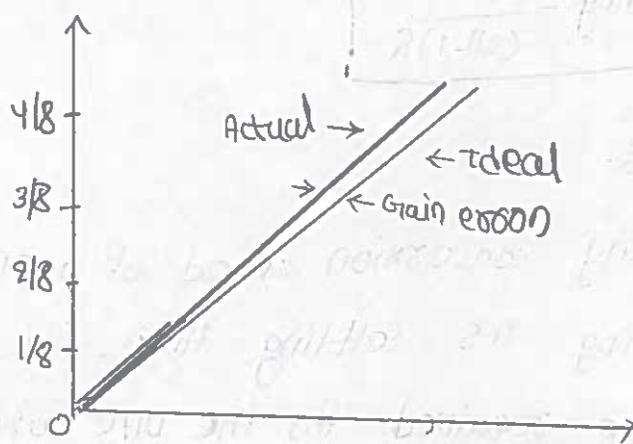


Fig:- Gain error in transfer characteristics of DAC

7. Non-linearity (Linearity Error) :-

An ideal DAC should be linear. For an ideal DAC, the output voltage would be a linear function of the input code. But it is fact that all DAC deviate somewhat from the ideal linearity.

8. Stability :-

The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

9. Monotonicity :-

A converter is said to have good monotonicity if it does not miss any step backward when stopped through its either range by a counter.

Basic DAC Techniques

3

There are mainly two techniques used for D/A conversions.

- Binary weighted resistor D/A converter.
- R/2R ladder D/A converter.

In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch position controlled by the digital IP & then converted into voltage to give analog voltage equivalent to be digital input.

1. Binary Weighted Resistor D/A converter :-

The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors $R, 2R, 4R, 8R, \dots, 2^{n-1}R$.

In the below figure switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage V_R ; otherwise it leaves resistor open. Therefore,

$$\text{FOR ON - Switch } I = \frac{V_R}{R} \text{ and}$$

$$\text{FOR OFF - Switch } I = 0$$

Here, operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through R_F .

Hence, the total current through R_F can be given as

$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

The output voltage is the voltage across R_F and it is given as

$$V_o = -I_T R_F = -(I_1 + I_2 + I_3 + \dots + I_n) R_F$$

$$= -\left[b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right] R_F$$

$$= -\frac{V_R}{R} R_F (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

when $R_F = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

The equation indicates that the analog output voltage is proportional to the input digital word.

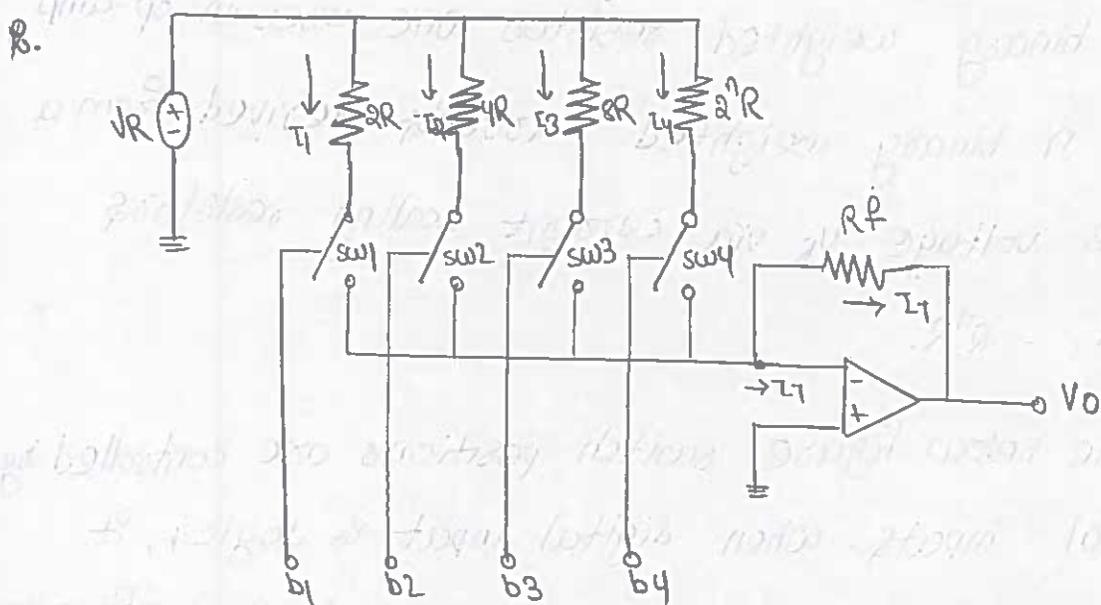


Fig:- Binary weighted resistor DAC

8. R-2R ladder DAC converter

(Voltage switching Mode)

In this type, reference voltage is applied to one of the switch positions, and other switch position is connected to ground, as shown in below.

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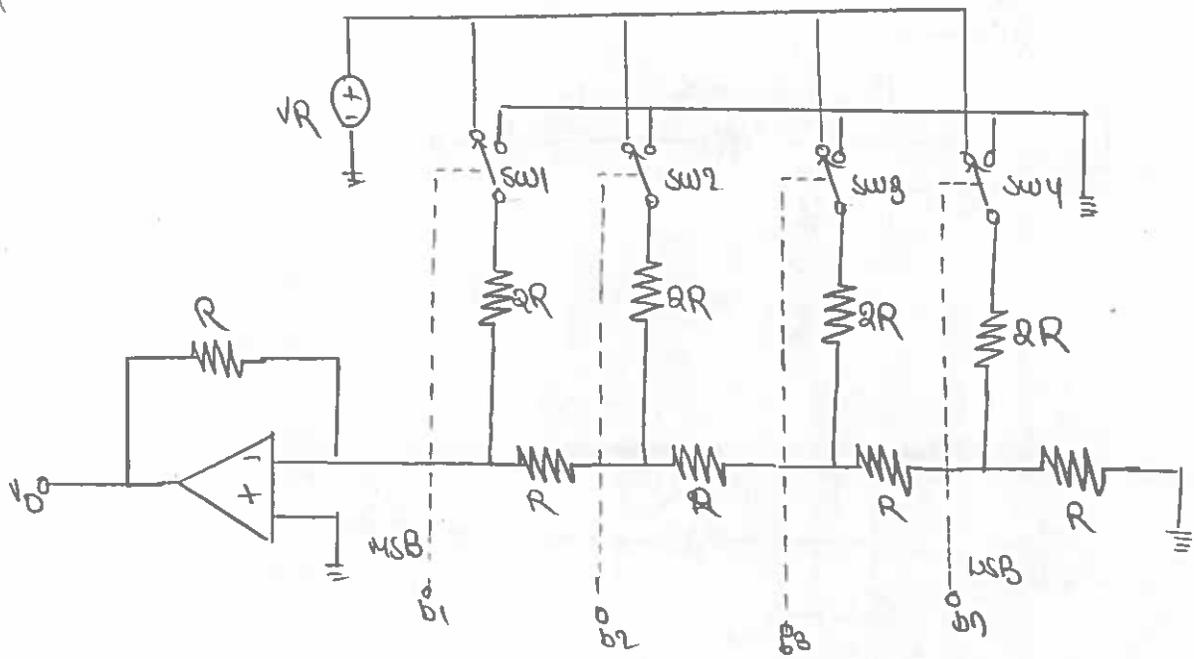


fig:- R/2R ladder DAC converter

let us consider 8-bit R/2R ladder DAC with binary input 001, as shown in the fig.

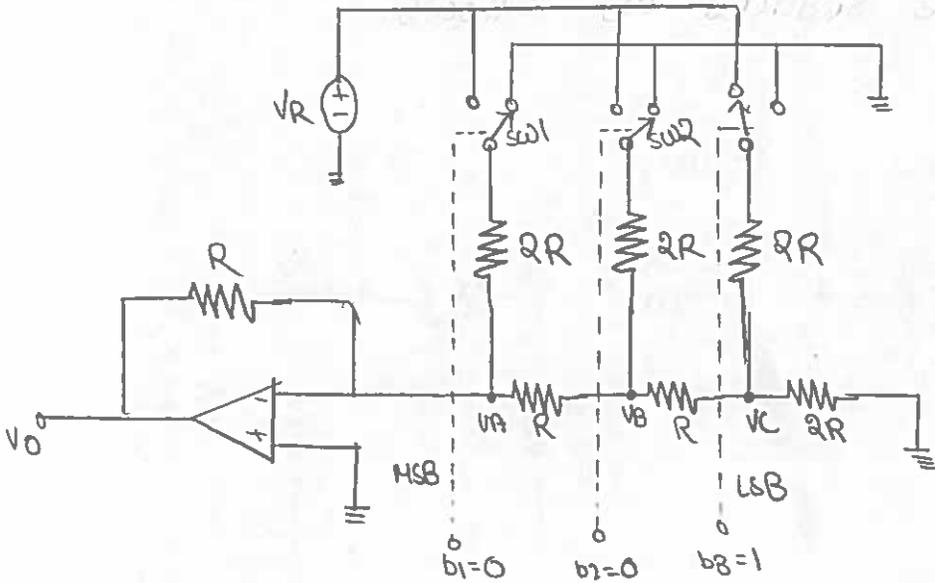
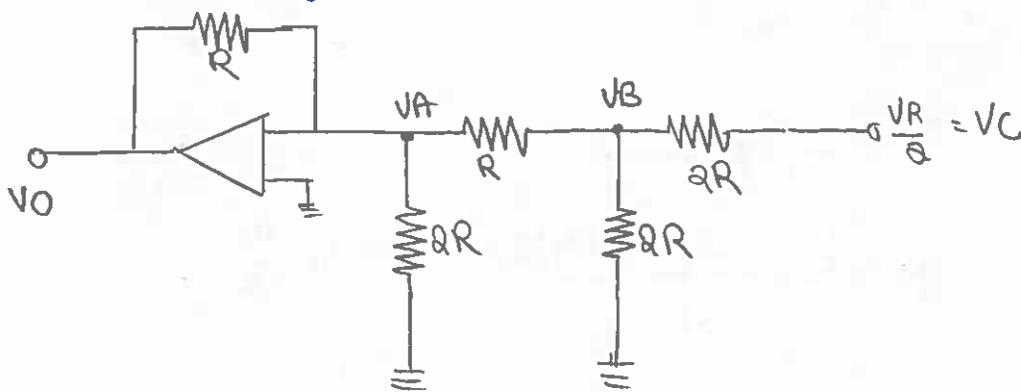


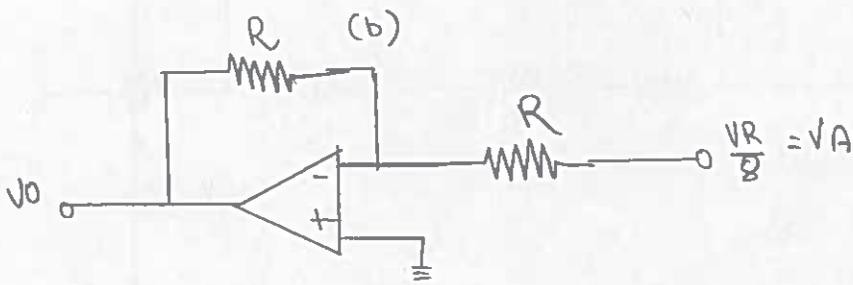
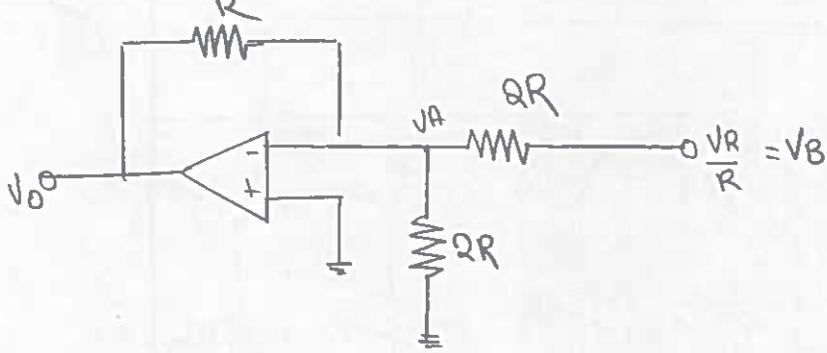
fig:- 3 bit R/2R ladder DAC

Reducing above network to the left by Thevenin's theorem we get,



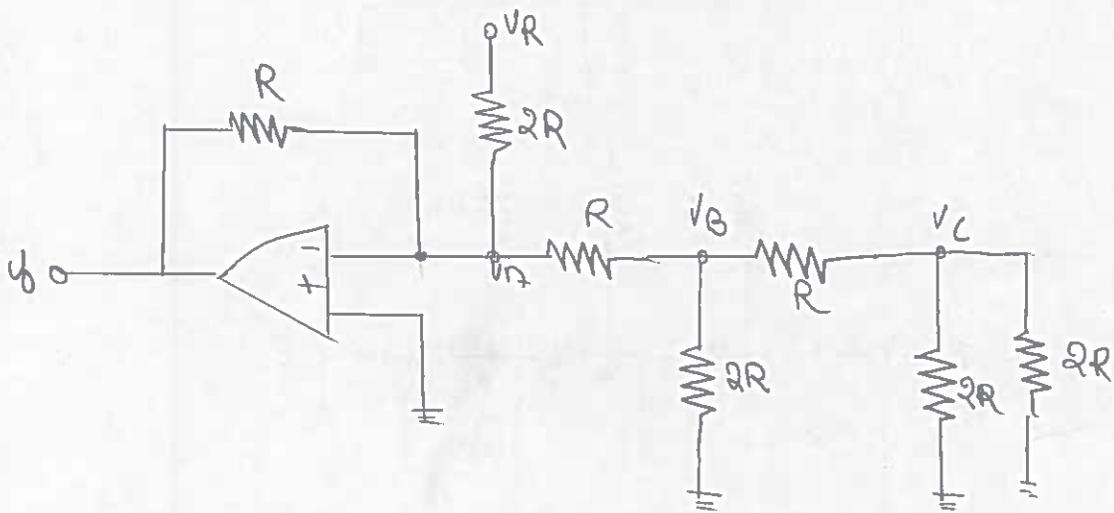
(a)

unit - 5, 7/26

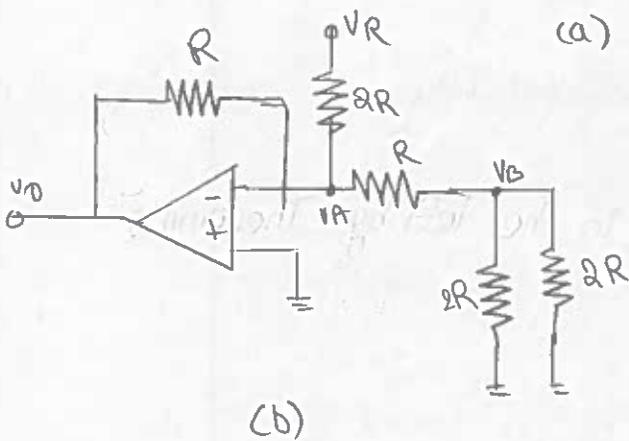


(c)

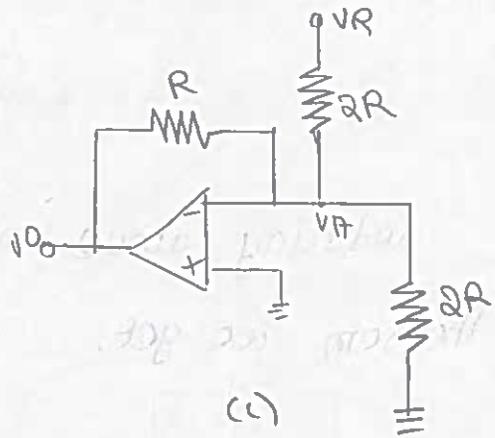
Therefore, the output voltage is $V_A/2$ which is equivalent to binary input 001. For binary input 100 the network can be reduced as follows.



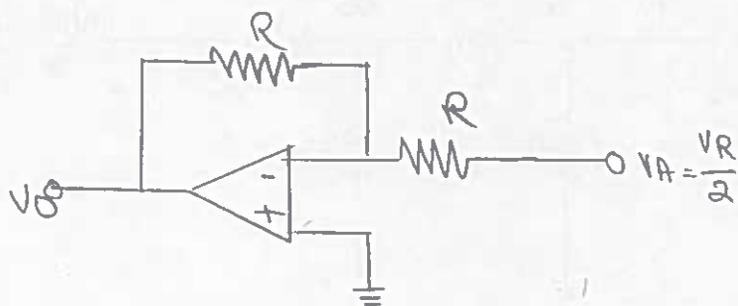
(a)



(b)



(c)



(d)

Therefore, the output voltage is $V_R/2$ which is equivalent to binary input 100. In general, the voltage is given by

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

3. Inverted R1R ladder DAC converted

(Current steering Mode)

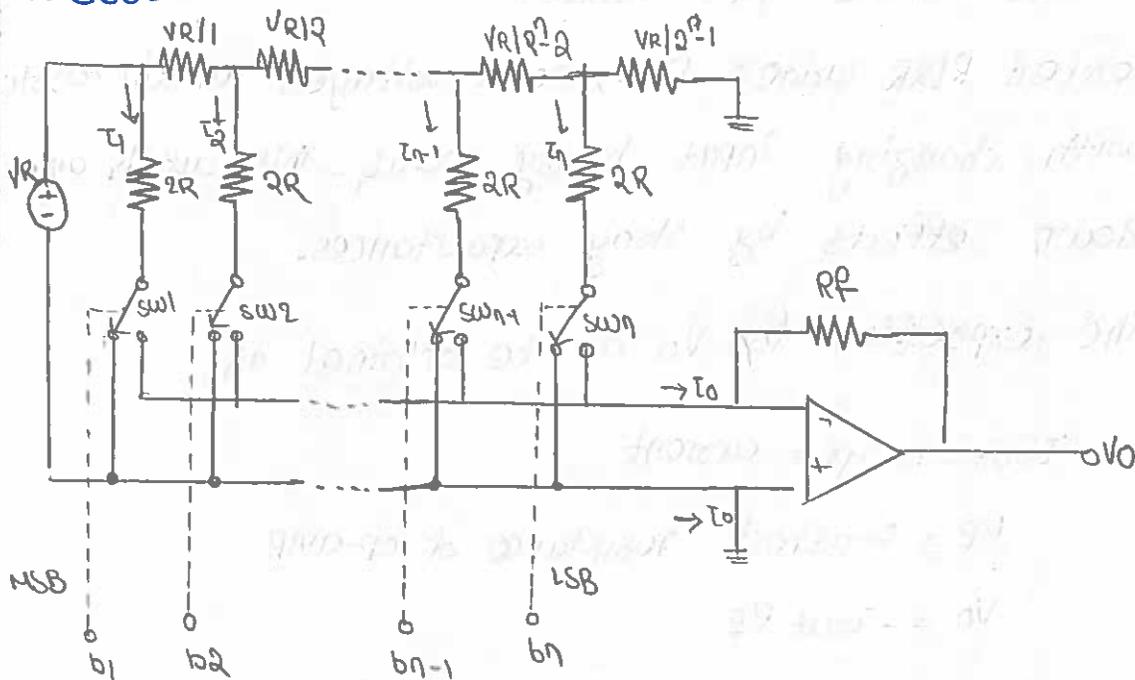
* R1R ladder DAC converted uses any only two resistor values.

* This avoids resistance spread drawback of binary weighted DAC converted, R1R ladder DAC.

* Like binary weighted resistor DAC, it also uses shunt resistors to generate n binary weighted currents.

* However, it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC.

* Voltage scaling requires an additional set of voltage dropping series resistance between adjacent nodes.



$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

we know that, V_o is given as,

$$V_o = -I_1 R_F$$

$$V_o = -R_F (I_1 + I_2 + I_3 + \dots + I_n)$$

$$= -R_F \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right)$$

$$= -\frac{V_R R_F}{R} (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

when $R_F = R$, V_o is given as,

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

Advantages of R/2R ladder DAC's

- 1, Easier to build accurately as only two precision metal film resistors are required.
- 2, number of bits can be expanded by adding more sections of same R/2R values.
- 3, In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

The expression for V_o can be obtained as,

Let I_{out} = output current

R_F = Feedback resistance of op-amp

$$V_o = -I_{out} R_F$$

Now I_{out} = current resolution $\times D$

$$\therefore V_o = - (\text{Current resolution} \times D) R_f$$

$$\therefore V_o = - (\text{Current resolution} \times R_f) D$$

The coefficient of D is the voltage resolution and can be called as simple resolution.

$$\therefore V_o = - \text{Resolution} \times D$$

In terms of actual circuit elements, output can be written as,

$$V_o = - \left(\frac{V_R}{R} \times \frac{1}{2^n} R_f \right) \times D$$

The resolution of R/R ladder type DAC with current output i_a ,

$$\text{Resolution} = \frac{1}{2^n} \times \frac{V_R}{R}$$

while the resolution for R/R ladder type DAC with voltage output v_a ,

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R} \right) \times R_f.$$

IC 1408 DAC :-

- The 1408 is an 8 bit R/R ladder type DAC converter compatible with TTL and CMOS logic.
- It is designed to use where the output current i_a linear product of an eight bit digital word.
- The IC 1408 consists of a reference current amplifier, an R/R ladder and eight high speed current switches.
- It has eight input data lines A_1 (MSB) through A_8 (LSB) which control the positions of current switches.
- It requires a mA reference current for all full scale input and two power supplies $V_{CC} = +5V$ and $V_{EE} = -15V$ (V_{EE} can range from $-5V$ to $-15V$)

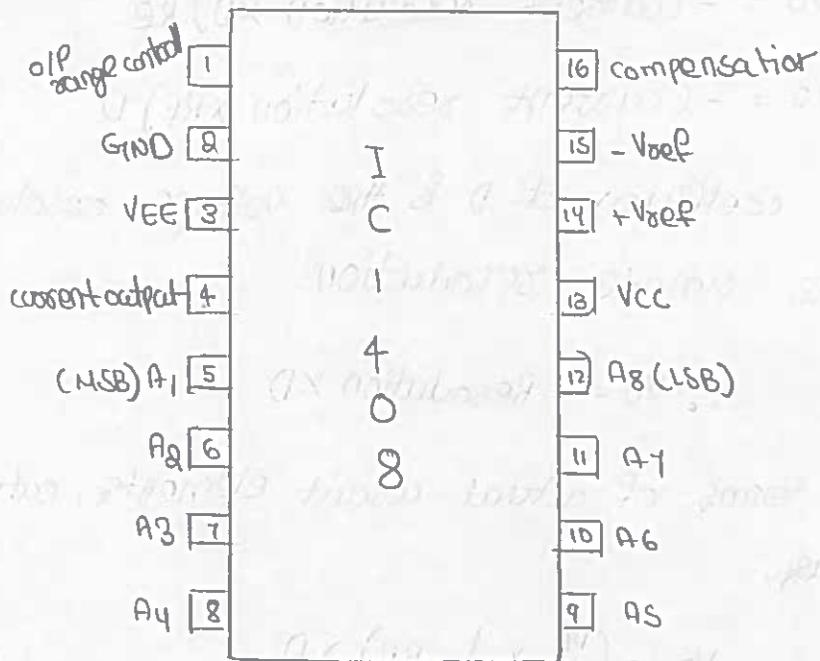


Fig. 2 - PIN Diagram

- The voltage V_{ref} and resistor R_{14} determines the total reference current source and R_{15} is generally equal to R_{14} to match the input impedance of the reference current amplifier.

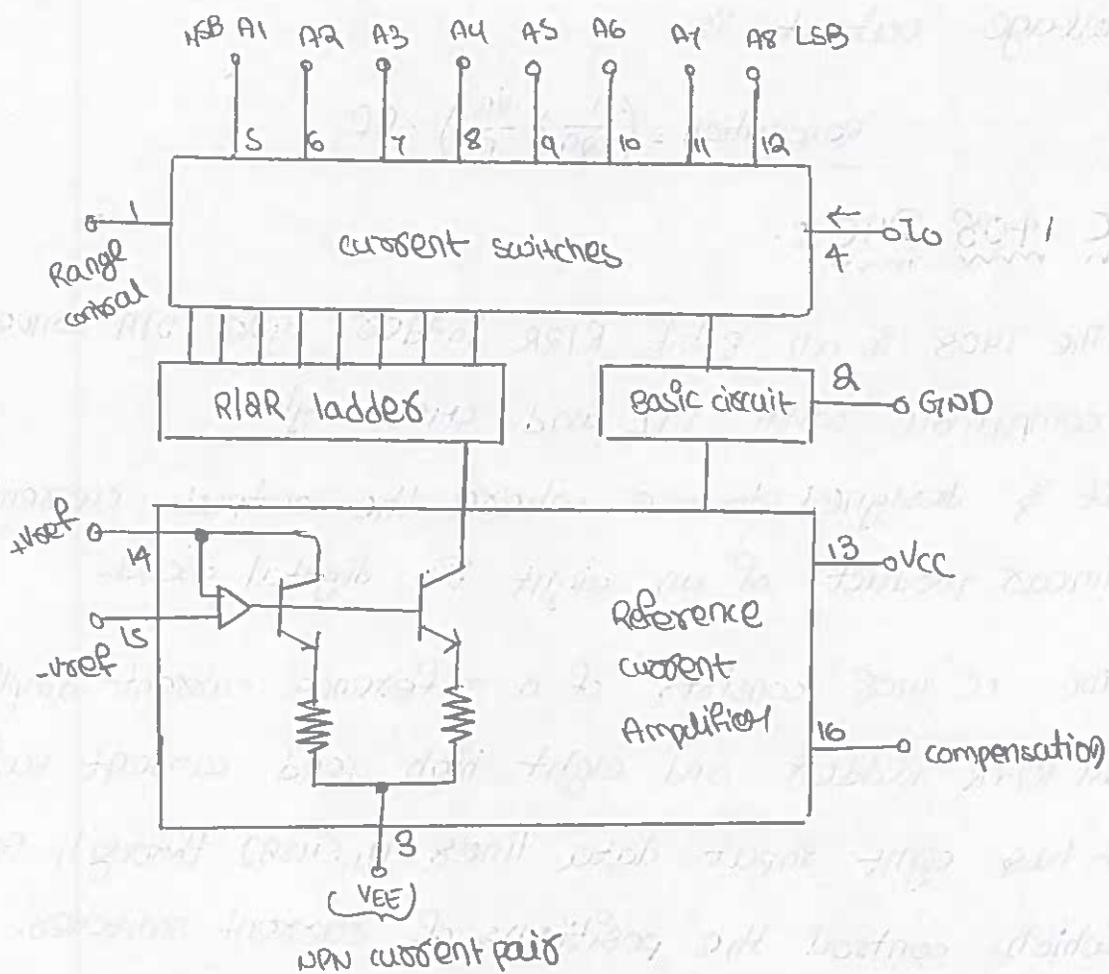


Fig. 3 - Block Diagram

- Shows a typical circuit for IC 1408. The output current I_o can be given as.

$$I_o = \frac{V_{ref}}{R_{14}} \left(\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right)$$

Note :-

Input A_1 through A_8 can be either 0 or 1. Therefore, for typical circuit full scale current can be given as,

$$I_o = \frac{5}{2.5K} \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right)$$

$$I_o = \frac{2mA \times 255}{256} = 1.992 mA$$

Important Electrical Characteristics for IC 1408 :-

- Reference current : 2 mA
- Supply voltage : +5 Vcc and -15V Vee
- settling time : 300ns
- Full scale output current : 1.992 mA
- Accuracy : 0.19%

Analog to Digital Converters

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function to that of the D/A converter.

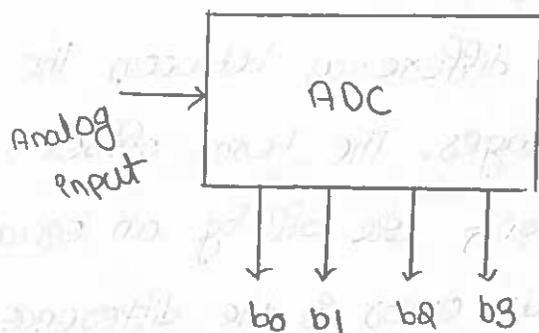


Fig:- symbol for 4-bit ADC

Performance parameters (specifications) of ADC :-

The digital output of an ideal 3 bit ADC plotted against the analog input voltage. Let us define the performance parameters of ADC.

1. Resolution :-

Resolution is defined as the ratio of a change in value of input voltage, V_i , needed to change the digital output by 1 LSB. If the full scale input voltage required to cause a digital output of all 1's is V_{iFS} , then resolution can be given as.

$$\text{Resolution} = \frac{V_{iFS}}{2^n - 1}$$

2. Quantization Error :-

There is an unavoidable uncertainty about the exact value of V_i when the output is 001. This uncertainty is specified as quantization error. Its value is $\pm \frac{1}{2}$ LSB.

$$Q.E = \frac{V_{iFS}}{(2^n - 1) \cdot 2}$$

quantization noise

$$E_n = \frac{V_{iFS}}{2^n \sqrt{12}}$$

3. Gain and Offset Error :-

The offset error is the difference between the actual and ideal first transition voltages. The term offset; however, implies that all conversions are off by an equal amount. On the other hand, the gain error is the difference between the actual full scale transition voltage and the ideal full-scale transition voltage.

4. Gain and offset Drifts :-

The gain drift is defined as a change in the full-scale transition voltage measured over the entire operating temperature range. It is usually expressed in parts per million per degree Celsius (PPM/°C).

The offset drift is defined as a change due to temperature in the analog zero for an ADC converter operating in bipolar mode. It is also expressed in parts per million per degree Celsius (PPM/°C).

5. Sampling Frequency and Aliasing Phenomenon :-

According to sampling theorem, the maximum rate at which the analog signal should be sampled twice the highest frequency in the analog signal.

$$f_s \geq 2f_{max}$$

The frequency of aliased signal is the difference b/w the signal frequency and the sampling frequency. This problem is called aliasing and it is removed in all practical ADC converters by using anti-aliasing filters.

6. Non-linearity or integral non-linearity (INL) :-

It is a measure of the maximum deviation of the actual ADC transfer function from a straight line drawn through the first and last code transition after correction for offset and gain errors.

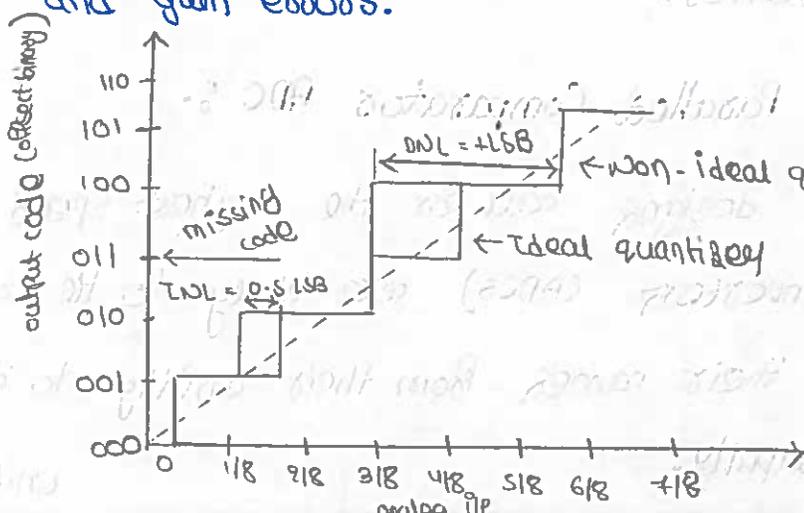


Fig. - INL & DNL analog ip

7. Differential Non-linearity (DNL) :-

Differential non-linearity (DNL) is the maximum of the difference in the each conversion's current code width (CCW) and the Ideal Code width (ICW).

DNL is the most critical of the measure of an ADC's performance for many applications.

$$DNL = CCW - ICW$$

$$DNL = \text{Max}(\text{code DNL})$$

8. Conversion Time (Settling Time) :-

It is the important parameter for ADC. It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used and the propagation delay of circuit components.

$$x_{\text{out}} \leq \epsilon$$

Different Types of ADC's

1. single RAMP or single slope
2. Dual slope
3. Successive Approximation
4. Flash
5. Counter type
6. Tracking converter.

⇒ Flash ADC or Parallel Comparator ADC :-

When system designs call for the highest speed available, flash-type A/D converters (ADCs) are likely to be the right choice. They get their names from their ability to do the conversion very rapidly.

* flash type A/D converters, also known as a simultaneous or parallel comparator ADC, because the fast conversion speed is accomplished by providing $2^n - 1$ comparators & simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

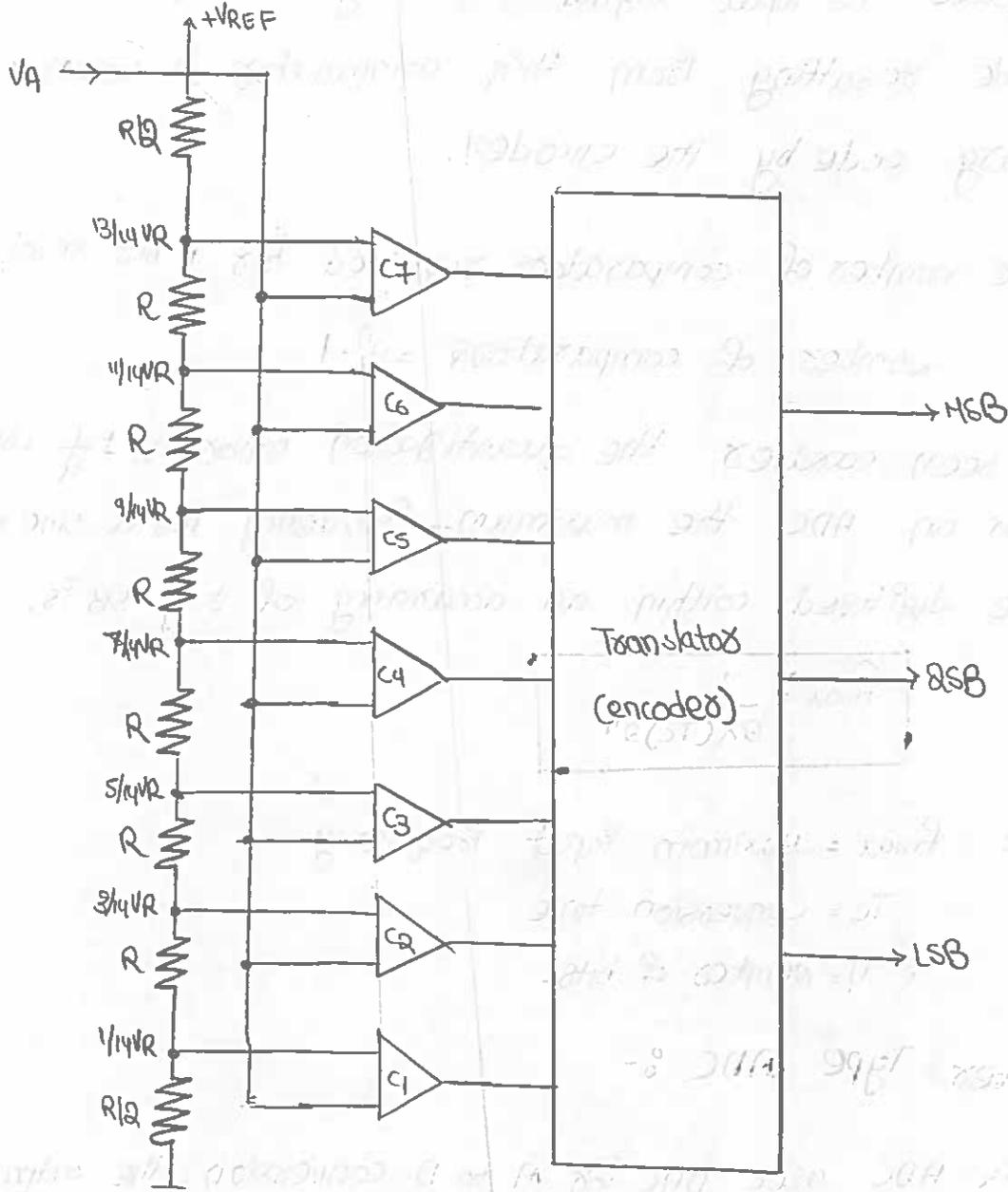


Fig 8 - Flash Converter

* 3 bit flash ADC for this ADC, seven ($2^3 - 1$) comparators are required.

* The reference voltage (V_{REF}) is equal to the full scale input signal voltage. The manner in which the flash A/D converter performs a quantization is relatively simple.

- * The comparators give output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant.
- * Those comparators referred above the input signal, remain turned -off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state.
- * The code resulting from this comparator is converted to binary code by the encoder.

The number of comparators required for n bit resolution is,
 number of comparators = $2^n - 1$

As seen earlier the quantization error is $\pm \frac{1}{2}$ LSB. Thus for an ADC, the maximum frequency for a sine wave V_{in} to be digitized within an accuracy of $\pm \frac{1}{2}$ LSB is,

$$f_{max} = \frac{1}{2^n (T_c) 2^n}$$

where f_{max} = Maximum input frequency
 T_c = Conversion time
 n = number of bits.

⇒ Counter Type ADC :-

* This ADC uses DAC for A to D conversion. The output of the DAC is continuously compared with the analog input to the ADC which is to be converted into digital output.

* When the output of the DAC becomes greater than this analog input, the corresponding digital input to the DAC is noted which represents the analog input to the ADC.

* The counter type ADC consists of a binary counter, DAC, comparator and AND gate. The operation of the circuit is explained below.

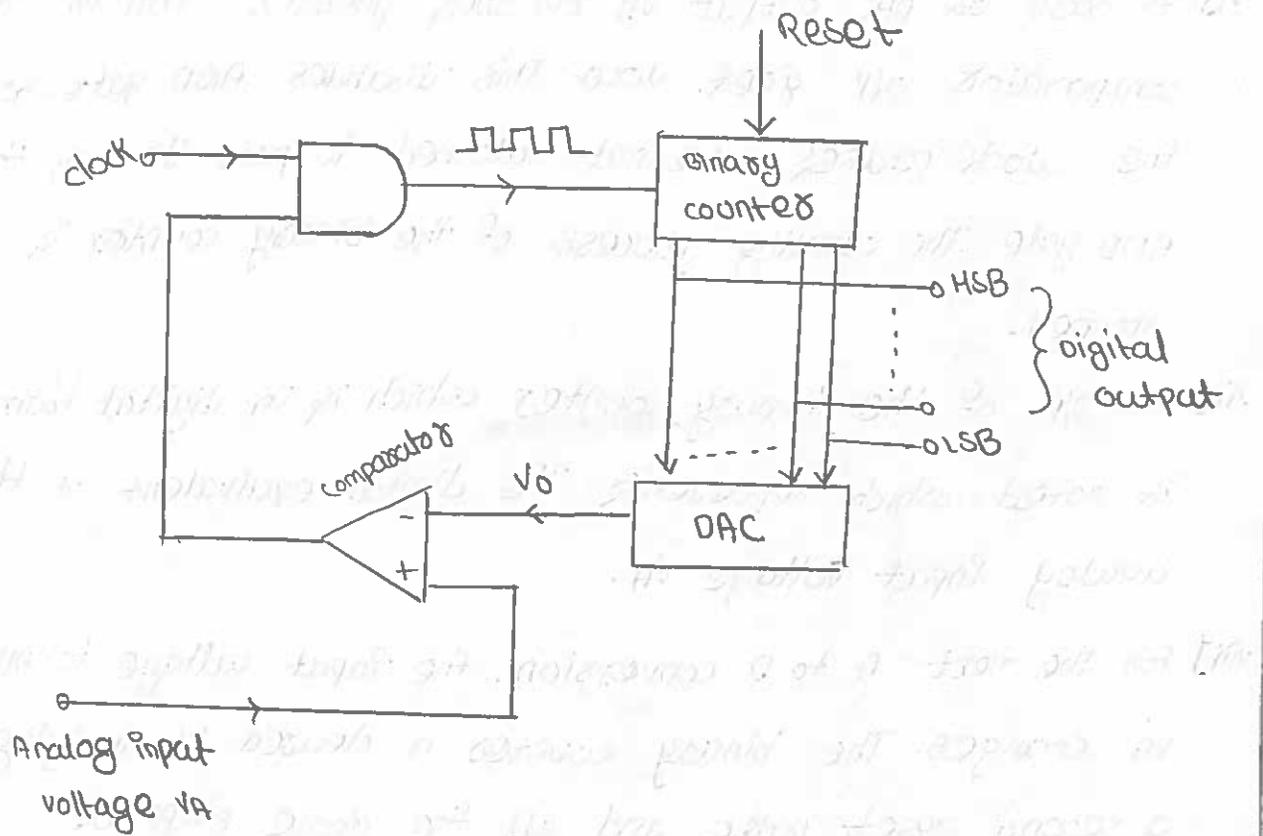


Fig 8- counter Type ADC

- i] Initially, the counter is reset, i.e., its output is set to zero by applying a reset pulse. The o/p of the counter is given as digital i/p to DAC. Since i/p to DAC is zero, its o/p V_0 is zero.
- ii] When the analog input voltage V_A is applied to DAC, it becomes greater than V_0 . V_A acts as input voltage for non inverting terminal and V_0 acts as input voltage for inverting terminal of the comparator output goes high.
- iii] For an AND gate, one input is clock pulses and another input is the output of the comparator. Because of the high output of the comparator, the clock pulses are allowed to pass through the AND gate.
- iv] The counter starts counting these clock pulses. According to the number of clock pulses, the output of the counter goes on increasing. This increases the output of the DAC.
- v] The above steps are continued till V_0 is less than V_A .

vii] As soon as DAC output V_0 becomes greater than V_A , the comparator's op goes low. This disables AND gate. So the clock pulses are not allowed to pass through the AND gate. The counting process of the binary counter is stopped.

viii] The op of the binary counter which is in digital form is noted which represents the digital equivalent of the analog input voltage V_A .

ix] For the next A to D conversion, the input voltage to ADC, V_A changes. The binary counter is cleared by applying a second reset pulse and all the above steps are repeated to obtain the digital equivalent of V_A .

⇒ Successive Approximation ADC :-

- In this technique, the basic idea is to adjust the DAC's ip code such that its op is within $\pm 1/2 \text{ LSB}$ of the analog input V_i to be A/D converted.
- The code that achieves this represents the desired ADC ckt.
- The successive approximation method uses very efficient code searching strategy called binary search. It completes searching process for n -bit conversion in just n clock periods.
- The external clock input sets the internal timing parameters. The control signal start of conversion (SOC) initiates an A/D conversion process and end of conversion signal is activated when the conversion is completed.

• Operation :-

- * The searching code process in successive approximation method is similar to weighing an unknown material with a balance scale and a set of standard weights.

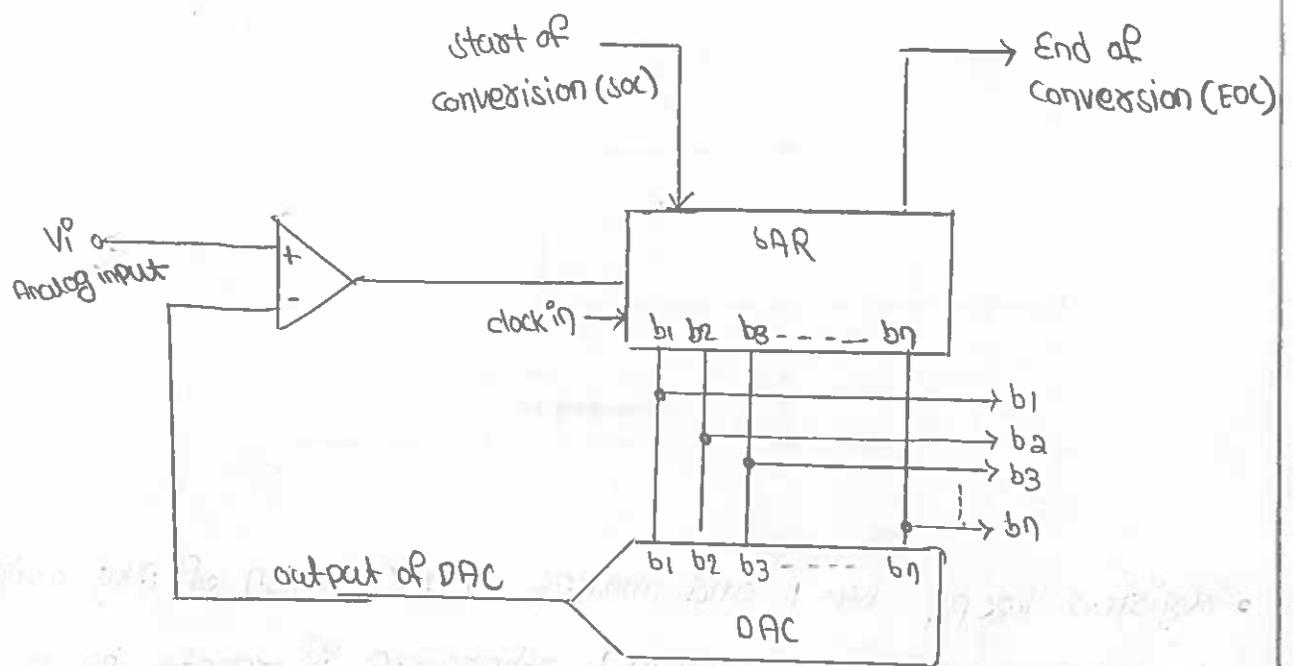
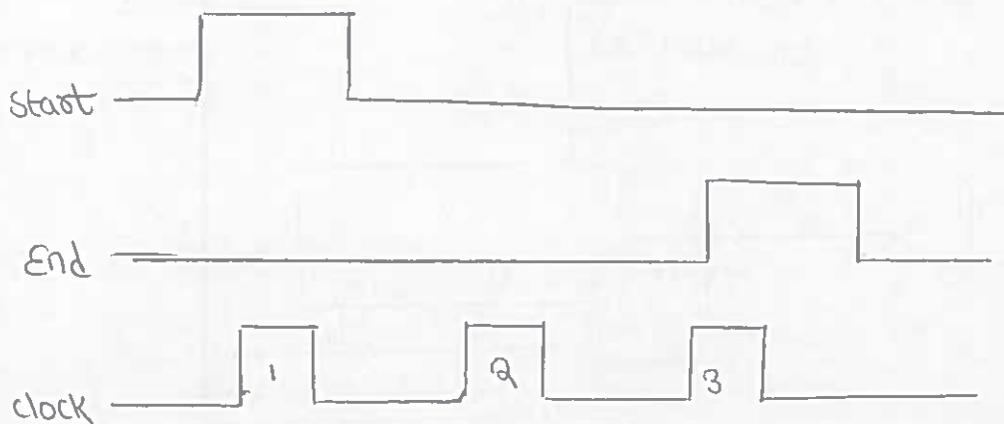


Fig:- Block diagram of successive Approximation ADC converter

- Let us assume that we have 1 kg, 2 kg and 4 kg weights (SAR) plus a balance scale (Comparator and DAC). Now we will see the successive approximation analogy for 3-bit ADC.
- The analog voltage V_i is applied at one input of comparator.
- On receiving start of conversion signal (SOC), successive approximation register sets 3-bit binary code (000 (b₂=1)) as an input of DAC.
- This is similar process of placing the unknown weight on one platform of the balance and 4 kg weight on the other.
- The comparator then compares two voltage just like comparing unknown weight with 4 kg weight with the help of balance scale.
- If the input voltage is greater than the analog output of DAC, successive approximation.



- register keeps $b_2=1$ and makes $b_1=1$ (addition of 2kg weight to have total 6kg weight) otherwise if resets $b_2=0$ and makes $b_1=1$ (replacing 2kg weight).
- The same process is repeated for b_1 and b_0 .

The time for one analog to digital conversion must depend on both the clock's period T and number of bits n . It is given as.

$$T_c = T(n+1)$$

T_c = conversion time

T = clock period

n = number of bits

⇒ Dual slope ADC :-

- * dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator, and then measured by a counter.
- * The speed of the conversion is slow but the accuracy is high.
- * It consists of integrator, comparator, binary counter, output latch and reference voltage.

- The Ramp generator input is switched between the analog input voltage V_i and a negative reference voltage, $-V_{REF}$.
- The analog switch is controlled by the MSB of the counter.
- When the MSB is a logic 0, the voltage being measured is connected to the ramp generator input.
- When MSB is logic 1, the negative reference voltage is connected to the ramp generator.

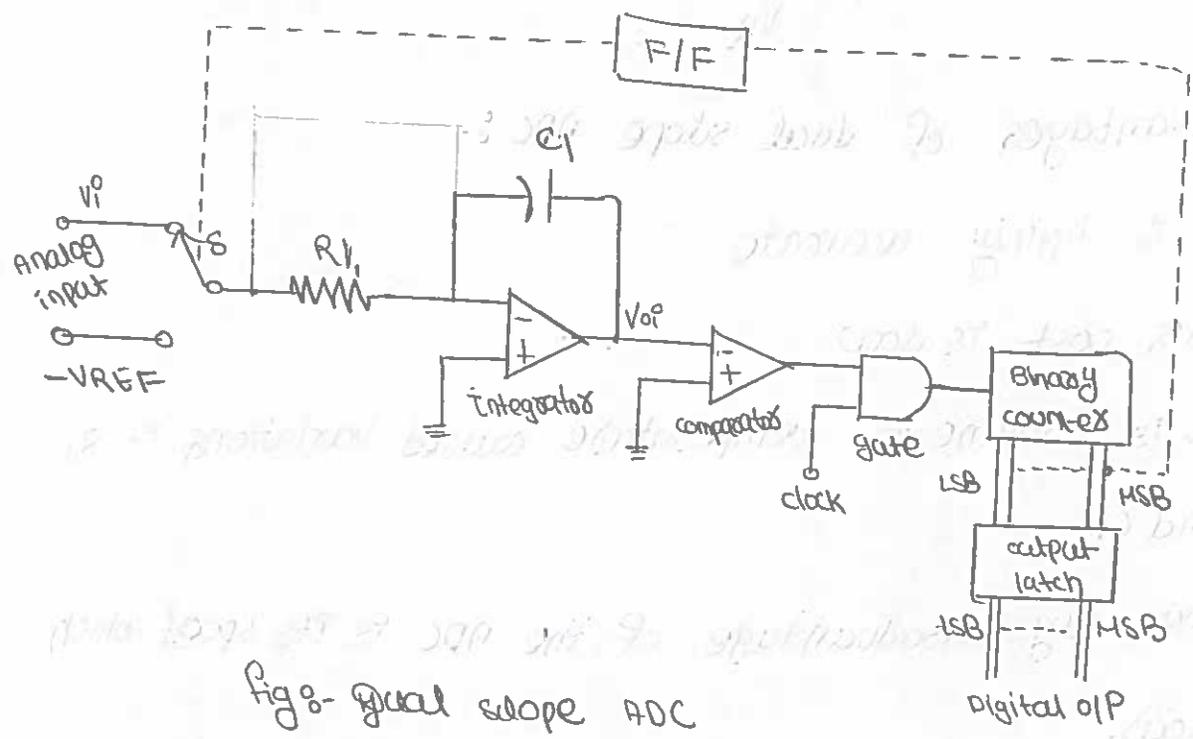


Fig:- Dual slope ADC

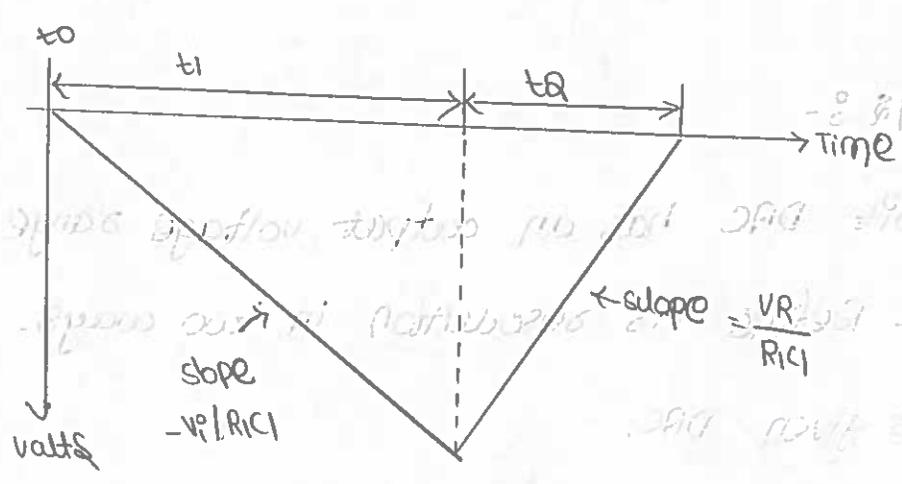


Fig:- Integrator's output voltage

The output voltage of the integrator can be

given as,

$$V_{oi} = -\frac{1}{R_i C_i} \int_0^t V_i dt = -\frac{V_i t}{R_i C_i}$$

The integrator's output ramp down to a voltage V and get back up to 0. Therefore, the charge voltage

is equal to discharge voltage and we can write,

$$\frac{Vt_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$\therefore Vt_1 = V_R t_2$$

$$\therefore t_2 = \frac{Vt_1}{V_R}$$

Advantages of dual slope ADC :-

⇒ It is highly accurate

⇒ It's cost is low

⇒ It is immune to temperature caused variations in R_1 and C_1

The only disadvantage of the ADC is its speed which is slow.

Problems :-

Q) An 8 bit DAC has an output voltage range of

0-2.55V. Define its resolution in two ways.

Sol For given DAC,

$$n = \text{number of bits} = 8$$

$$? \text{ Resolution} = 2^n = 2^8 = 256$$

i.e., the output voltage can have 256 different

values including zero.

1) $V_{OFS} = \text{Full scale output voltage} = 2.55V$

$\therefore \text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{2.55}{2^8 - 1} = \frac{10mV}{1LSB}$

2) Find out stepsize and analog output for 4 bit R-2R ladder DAC when input is 1000 and 1111. Assume

$V_{REF} = +5V$

Sol For given DAC,

$n = 4, V_{OFS} = +5V$

$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{5}{2^4 - 1} = \frac{1}{3} V/LSB$

$\therefore V_o = \text{Resolution} \times D$

For $D = \text{Decimal of } (1000)_2 = 8$

$V_o = \frac{1}{3} \times 8 = 2.6667V$

For $D = \text{decimal of } (1111)_2 = 15$

$V_o = \frac{1}{3} \times 15 = 5V$

3) determine the resolution of an 8 bit ADC converter for a 10V input range.

Sol $V_{IFS} = 10V$

$R = \frac{V_{IFS}}{2^n - 1} = \frac{10}{2^8 - 1} = \frac{10}{255} = 39.215 mV$

4) An 8 bit successive approximation ADC is driven by a 1MHz clock. Find its conversion time.

Sol $f = 1MHz$

$\therefore T = \frac{1}{f} = \frac{1}{1 \times 10^6} = 1 \mu sec$

$$n = 8$$

$$\therefore T_C = T(n+1) = 1(8+1) = 9 \text{ } \mu\text{sec}$$

Q] For a particular dual slope ADC, t_1 is 88.88 ms and the reference voltage is 100mV. Calculate t_2 if V_i is 100mV and (ii) 200mV.

Sol we know that,

$$t_2 = \left[\frac{V_i}{V_R} \right] t_1$$

i] $t_2 = \left[\frac{100}{100} \right] (88.88) = 88.88 \text{ ms}$

ii] $V_i = 200 \text{ mV}$

$$t_2 = \left[\frac{200}{100} \right] (88.88) = 166.6 \text{ ms}$$

Q] For a particular 8 bit ADC, the conversion time is 9 μsec . And the maximum frequency of an input sine wave that can be digitized.

Sol

The maximum frequency is given by

$$f_{\text{max}} = \frac{1}{2^n T_C} = \frac{1}{2^8 \times 9 \times 10^{-6}} = 69.07 \text{ Hz}$$